International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 03 Issue: 11 | Nov -2019 ISSN: 2590-1892

DESIGN AND IMPLEMENTATION OF PAL AND PLA USING REVERSIBLE LOGIC

Dr.T.PEARSON, A.SAATHWIK REDDY, P.MAHESHWARI, G.APARNA

*Professor,St. Peter's Engineering College, Department of Electronics and Communication Engineering, Hyderabad, Telangana,India
**Scholar, St. Peter's Engineering College, Department of Electronics and Communication Engineering, Hyderabad, Telangana,India

ABSTRACT

Reversible logic is the emerging field for research in present era. The aim of this project is to design and synthesize a Programmable array Logic (PAL) and Programmable Logic array (PLA) using reversible logic with minimum quantum cost. The PAL is a Programmable Logic device which consists of programmable AND Gates and fixed OR gates array. The PLA is the PLD which contains programmable AND array andprogrammable OR array. The PLDs are the combinational circuits mainly used to realize Boolean functions onour interest. An n input and k output Boolean function f (a1, a2, a3, …., an) (referred as (n, k)) is said to be logically reversible if and only if, the number of inputs are equal to the number of outputs i.e., 'n' equals 'k'and the input pattern maps uniquely maps the output pattern. The reversible logic must run bothforward and backward in such a way that the inputs can also be retrieved from outputs. There are many reversible logic gates in literature like NOT gate, Feynman Gate (CNOT gate),Double Feynman Gate, Peres Gate, TR gate, SeynmanGateand many more. Fan-out and Feed-back are not allowed in Logical Reversibility.

To overcome the Fan out limitation, the signals from required output lines are duplicated to desired lines using additional reversible combinational circuits. Reversible Logic[1] owns its applications in various fields which include Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI etc.,

Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption and low heat dissipation. In this paper, the design of PAL and PLA[1] which has less heat dissipation and low power consumption is proposed. The designed circuits are analyzed in terms of quantum cost, garbage

outputs and number of gates. The Circuit has been designed and simulated using Xilinx software.

KEYWORDS:PAL, PLA, PLDS, Quantum Cost, Reversible Gates, Garbage Outputs, Number of gates.

INTRODUCTION

Inpresent VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible logic, power consumption and heat dissipation can be minimized[2]. Power consumption is very less in reversible logic circuits when compared to irreversible logic circuits. Reversible Logic finds its own application in Quantum computing, Nano-technology[3],Optical computing, Computer graphics and Low Power VLSI.

Ralf Launduer told that heat dissipation in irreversible circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the logical computation process. He demonstrated Launder's principle which describes the lower theoretical limit of heat dissipation in logical computation. Launder's principle states that losing a single information bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant (approximately 1.38×10-23 J/K), T is Temperature and ln2 is natural algorithm of 2 (approximately 0.69315). The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits. It is necessary to notice that there is a direct relationship between the numbers of information bits erased to the amount of heat dissipated in the circuit. Later in 1973 C. H. Bennett described that the Power dissipation due to the bit losscan be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the computation is carried out in reversible manner. He argued that for zero heat dissipation, the computation must be done in reversible manner. But if reversible logic is utilized to do logical computation, the heat dissipation[2] will be less than KTln2 for one information bit in contrast to Launder.Thus computation done in reversible matter doesn't require erasing of bits.

RESEARCHWORK

The Reversible Logic involves the use of Reversible Gates which consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vector lines and output vector lines. In reversible computation, the reversible gates are made to run both forward and backward directions. If the device obeys above two conditions, it satisfies the second law of

thermodynamics which preserves the information bits without getting erased and guarantees that no heat is dissipated**.** Certain limitations are to be considered when designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedbackis also not permitted in reversible logic[4]. In Reversible logic using outputs we can obtain full knowledge of inputs. To overcome the Fan-out limitation, by using additional reversiblecombinational circuits[5], the output lines are duplicated into required number of lines that are required to drive the inputs of consecutive device.Similarlyfor Feedback limitation delay elements are used. Reversible logic conserves information.

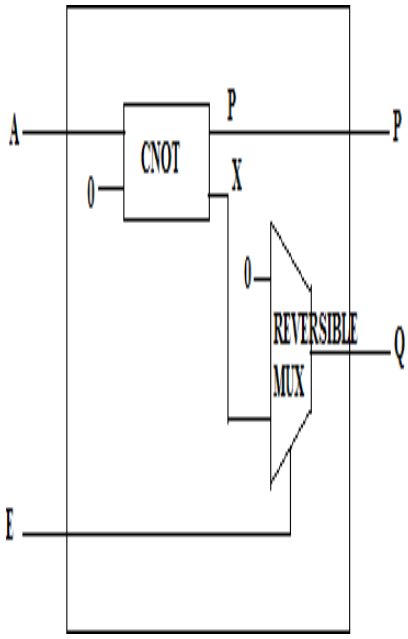
Some cost metrics like Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are kept alone without performing any operations. Number of gates count is not a good metric since more number of gates can be taken together to form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement a reversible logic gate. It is nothing but the number of reversible gates (1×1 or 2×2) required to construct the circuit. The quantum cost plays an important role in logical reversibility. If the quantum cost is more, then the area of the circuit increases, thereby increasing the propagation delay. But quantum cost doesn't impact heat dissipation. Delay is one of the important cost metrics. A Reversible circuit design can be modeled as a sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research.

In this paper the design of Programmable Array Logic (PAL) and Programmable Logic Array (PLA) using reversible logic with minimum Quantum cost is proposed.

PROPOSEDMETHOD

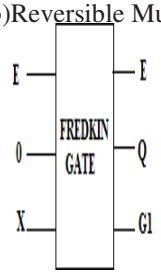
The Programmable Array Logic (PAL), Programmable Logic array (PLA) is realized using reversible Fredkingate and Feynman gate[6] as shown in the figure11 and figure12 respectively. The concept of duplicating a single output torequired number of outputs using Feynman gate is introducedwhere Fan-out was not allowed in reversible computation. Thestandard irreversible conventional PLDs can be programmed.

The irreversible PLDs consist of a series of fuses which can be burned to program the device. By burning the fuses, the chip can be programmed which is an irreversible process.



In reversible PLDs structure, the fuses are replaced with a reversible fuse which is made of reversible Feynman gate and Fredkin gate[6] as shown in the below figure. The Feynman reversible gate acts as a duplicating circuit. It duplicates the outputline into two output lines out of which one output line drives the next circuit and the other drives the second input of 2×1 reversible multiplexer. The first input of reversible multiplexer is grounded so that when the enable signal 'E' is low it acts as an 'off' switch.Thereversible multiplexer is made of Fredkingate as shown in the below figure.

(a) Reversible Fuse (b)Reversible Mux



The fixed connections are replaced by CNOT gates in which the second input is set to '0' always. The CNOT gates give solution for two remedies. It overcomes the feedback limitation and it acts as a fixed connection. The Design of PAL made of reversible logic[4] which is programmed toper form the operation of the below Boolean algebraic equations is shown in the below figure. The PAL consists of fixed OR gates array and programmable AND gatearray.

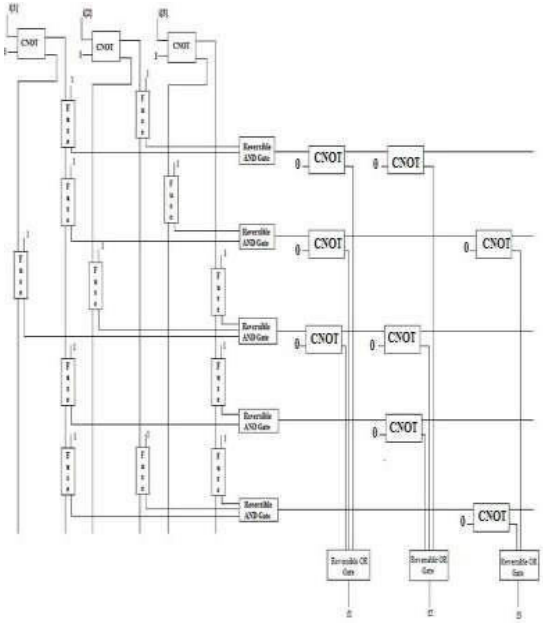


Fig1:Circuit diagram of Reversible PAL to perform Boolean algebraic equations operation.

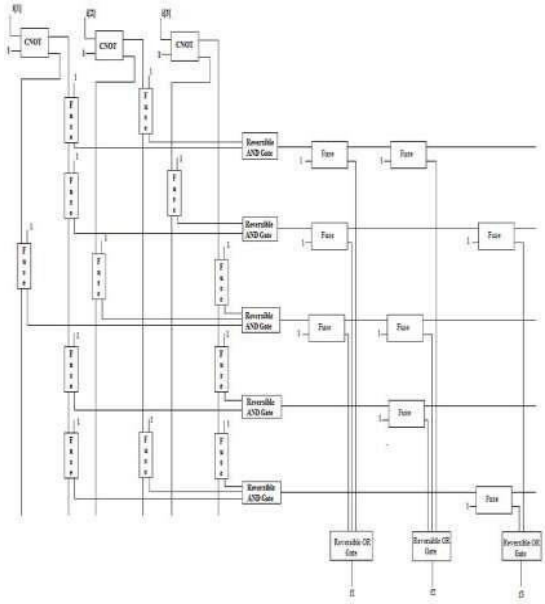


Fig2: Circuit diagram of Reversible PLA to perform Boolean algebraic equations operation.

Eqn(1)

F2 = I[1]I[2] + I[1]'I[2]'I[3]+I[1]I[3].....Eqn(2)
F3 = I[1]I[3]'+I[1]I[2]I[3]……Eqn(3)

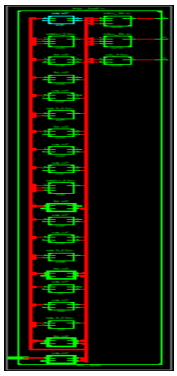


Fig3: RTL Schematic of PAL implementing using reversiblelogic gates

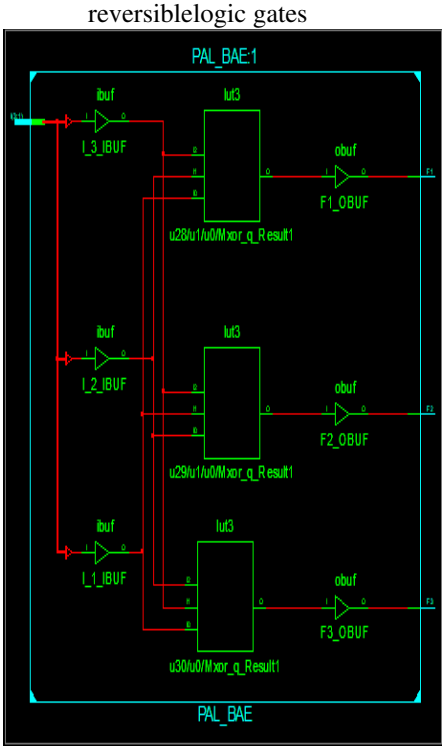


Fig4: Technology schematic of proposed PAL

SIMULATION RESULTS ANDCOMPARISION

1.REVESIBLE PROGRAMMABLE ARRAYLOGIC

The RTL schematic and simulated [7] output for Eqn1 to Eqn3 implemented using reversible PLA is shown in the figure and figure respectively.

F1=I[1]I[2]+I[1]I[3]'+I[1]'I[2]'I[3]

.....

PAL_BAE Project Status (09/22/2018 - 09:12:19)			
Project File:	code_39.xise	Parser Errors:	No Errors
Module Name:	PAL_BAE	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	
Product Version:	ISE 14.4	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	4656	0%
Number of 4 input LUTs	3	9312	0%
Number of bonded IOBs	6	232	2%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Sep 22 09:14:47 2018			
Translation Report					
Map Report					
Place and Route Report					

Fig5: design utilization summary of proposed PAL

Fig6: simulation output of proposed PAL synthesized and simulated using XILINX 14.4 design suit.

2.REVERSIBLE PROGRAMMABLELOGICARRAY

The equations Eqn1 to Eqn3 are implemented using reversible PLA. The RTL schematic[7] implemented using reversible PLA is shown in the figure respectively.

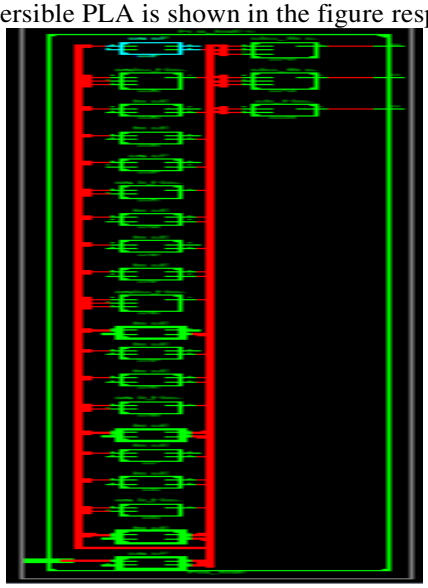
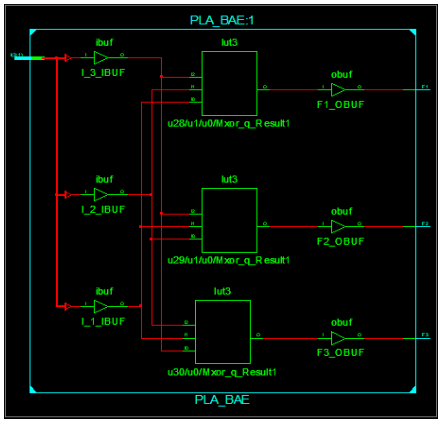


Fig7: RTL Schematic of PLA implementing using reversible logic gates

Fig8: Technology schematic of proposed PLA



PLA_BAE Project Status			
Project File:	code_39.xise	Parser Errors:	No Errors
Module Name:	PLA_BAE	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	
Product Version:	ISE 14.4	• Warnings:	
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	4656	0%
Number of 4 input LUTs	3	9312	0%
Number of bonded IOBs	6	232	2%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Sep 22 09:14:47 2018			
Translation Report					
Map Report					
Place and Route Report					

Fig9: Design utilization summary of proposed PLA

Fig10: Simulation output of proposed PLA

CONCLUSION

In this paper, the method of realizing different Boolean functions using reversible PLDs like reversible PAL, reversible PLA are explained. These circuits are designed for minimum quantum cost and minimum garbage outputs. To overcome the fan-out limitation in reversible logic circuits the concept of duplicating the single output to required number of output lines is implemented by using additional reversible combinational circuits. The reversible PLDs are implemented using a reversible fuse and Feynman gate. The reversible fuse is made of CNOT gate and Fredkingate which is used for programmable connections. Feynman gate with second input made zero is used for fixed connections. The reversible circuits used for designing programmable connections and fixed connections give minimum heat dissipation.

By using this reversible PLDs eighty percentage of efficiency can be acquired in terms of heat dissipation. The time delay increases a little when compared to irreversible PLDs which can be termed as a disadvantage but it is negligible. The time delays for reversible PAL, PLA and GAL are 5.847nsec, 5.847nsec and 5.847nsec respectively. The time delay depends upon the Boolean expressions considered to program on the device. The time delay is the function of quantum cost. The quantum cost increases with increase in length of Boolean function,because the number of programmable reversible fuses and Feynman gates (fixed connectors) increases with increase in length of Boolean function. If quantum cost increases, the time delay also increases. The reversible PAL finds more advantages when compared to the reversible PAL and PROM[8], since both OR array AND arrayare Programmable. Because of using reversible decoder in PROM, the quantum cost becomes less when compared to the remaining PLDs.The propagation delay can be reduced if the quantum cost of the circuit is reduced further more. This can be termed as future scope for thispaper.

REFERENCES

[1] Kumar, D. and Swamy, T. (2016). VHDL Design and Implementation of C.P.U by Reversible Logic Gates. *International Journal of Advanced Scientific Technologies in Engineering and Management Sciences*, 2(12), p.108.

[2] Chakraborty, K. (2016). Design and Implementation of High-Speed Low Power Multipliers Using Reversible Logic. *International journal of Emerging Trends in Science and Technology*.

[3] Jadav. ChandraDas, Debashis. De, Tapatosh. Sadu, "A novel low power nano scale reversible decoder using nano communication", *Third International Conferrence on devices circuits and systems*, 2016.

[4] JN, R., AM, V. and S, M. (2018). Design and Implementation of Vedic Multipliers Using Reversible Logic Gates. *Journal of Electrical & Electronic Systems*, 07(02).

[5] Ritjit Maumdar, sandeep. saini, "A novel design of reversible 2: 4 decoder", *978-1-4799-6761-2\$31.00©2015 IEEE.* Gopi Chand Naguboina, Anusudha.k "Design and Synthesis of Combinational Circuits using Reversible decoder in Xilinx" International Conference on Computer Communication and Signal Processing, ICCCSP
17.chennai

[6] Bala Krishna, K. and Purna Ramesh, A. (2019). Implementation of sequential circuit using Feynman and Fredkin reversible logic gates. *Journal of Physics: Conference Series*, 1228, p.012047.

[7] B.L. Synthesis, V. GroupAbc:A System for Sequential Synthesis and Verification
(2017)

[8] H. Cai, Y. Wang, L.A.D.B. Naviner, W. ZhaoRobust ultra-low power non-volatile logic-in-memory circuits in fd-soi technology IEEE Transactions on Circuits and Systems I: Regular Papers, 64 (4) (2016), pp. 847-857